

REMARKS

The claims remaining in the present application are Claims 2-13, 16-20 and 22-24. Claims 2, 16-17, 19-20 and 22-23 have been amended. Claims 1, 14-15 and 21 have been cancelled, without prejudice. Claim 24 has been added. No new matter has been added as a result of these amendments.

35 U.S.C. §103

Claims 1-23 are rejected under 35 U.S.C. §102 as being unpatentable over Kleinsorge et al., U.S. Pat. No. 6,247,109 (hereinafter, Kleinsorge). Claims 1, 14-15 and 21 have been cancelled, without prejudice. Therefore, the rejection to these claims is rendered moot. The rejection to Claims 2-13, 16-20 and 22-23 is respectfully traversed for the reasons below.

Claim 2 recites:

A system having a partitioned memory, said system comprising:  
a plurality of processors;  
a hardware implemented memory router coupled to said processors; and  
memory coupled to said memory router;  
wherein said memory router is configured to store memory partition information describing the memory allocated to each of said plurality of processors; and  
wherein said memory router is further operable to map memory access requests from said plurality of processors to respective

addresses in said memory allocated to each of said plurality of processors.

Claim 2 recites a hardware implemented memory router. In contrast, Kleinsorge expressly teaches away from a hardware implemented memory router. Kleinsorge is concerned with scalability, which is Kleinsorge teaches is aided by use of software partitioning. “[T]he CPUs and other hardware are associated solely with software. Such a platform is inherently scalable.” (Kleinsorge col. 6, lines 57-59). Kleinsorge also teaches “This partitioning, which a system manager directs, is a software function; no hardware boundaries are required” (col. 4, lines 59-61). Thus, one would not be motivated to modify Kleinsorge to arrive at the claimed hardware router because Kleinsorge teaches that using software to partition is inherently scalable.

For the foregoing rationale, Claim 2 is not anticipated nor rendered obvious by Kleinsorge. As such, allowance of Claim 2 is respectfully solicited.

Currently Amended Independent Claim 16 recites:

A method of partitioning memory, said method comprising the steps of:

a hardware implemented memory router receiving a request for memory access from one of a plurality of processors, said request specifying a first address;

said hardware memory router determining the location in memory corresponding to said first address, said memory partitioned among said plurality of processors;

said hardware memory router routing said memory request to said memory, wherein said memory access is securely executed such that said one of said plurality of processors is only able to access memory which is allocated to it; and

re-partitioning said memory by re-configuring said hardware memory router with commands entered via an external port to said memory router, wherein software executing on said plurality of processors is unable to modify said memory router.

Claim 16 recites limitations of “re-partitioning said memory by re-configuring said hardware memory router with commands entered via an external port to said memory router, wherein software executing on said plurality of processors is unable to modify said memory router.”

Applicants respectfully assert that Kleinsorge fails to teach or suggest these limitations. In contrast, Kleinsorge teaches that a configuration tree is modified by software executing on one of the processors in the computer system. Thus, Kleinsorge fails to suggest the claimed external port, which allows commands for re-partitioning the memory by re-configuring the hardware router. Moreover, Kleinsorge requires that software on one of the processors in the computer system re-configure the configuration tree.

For the foregoing rationale, Claim 16 is not anticipated nor rendered obvious by Kleinsorge. As such, allowance of Claim 16 is respectfully solicited.

Currently Amended Claim 23 recites:

A hardware implemented memory router comprising:

an input to receive a memory access request, said request specifying an address in a first processor's of a plurality of processors address space;

a table for storing memory partition information, said information describing the memory allocated to each of said plurality of processors;

logic operable to translate said address in said processor address space to a corresponding address in said memory; and

a first component and a second component, said first and said second components coupled by a communication link, wherein said first component is operable to add a key to said address specified by said processor request, said key identifying the processor of said plurality making said request; and wherein said second component is operable to use said key to route said request to the appropriate memory address, wherein multiple processors using the same communication link and using overlapping processor addresses securely access said memory (emphasis added).

Kleinsorge fails to teach or suggest the underscored claim limitations involving the key. Kleinsorge teaches that all of the processors may address all of the available memory (col. 6, lines 50-54). However, Kleinsorge is silent as to adding a key to an address specified by a

processor request. Moreover, Kleinsorge fails to teach or suggest multiple processors using the same communication link and using overlapping processor addresses while securely accessing memory, as claimed.

Claims 3-13, 17-20, and 22 depend from Claims 1, 16, and 23, which are believed to be allowable for the foregoing reasons. As such, Claims 3-13, 17-20, and 22 are believed to be allowable and their allowance is earnestly solicited.

NEW CLAIM

Claim 24 has been added. Support for new claim 24 may be found in the instant specification at least at page 11, lines 13-21. No new matter as been added. Claim 24 is respectfully believed to be allowable at least by virtue of its dependency from Claim 23, which is believed to be allowable for reasons discussed herein.

